



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

10/526,689

03/03/2005

Yong-Ho Yang

8054-92 (LW8052PC/US)

5285

22150 7590 04/14/2009
F. CHAU & ASSOCIATES, LLC
130 WOODBURY ROAD
WOODBURY, NY 11797

EXAMINER

SCHECHTER, ANDREW M

ART UNIT

PAPER NUMBER

2871

MAIL DATE

DELIVERY MODE

04/14/2009

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/526,689	Applicant(s) YANG ET AL.	
	Examiner ANDREW SCHECHTER	Art Unit 2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 04 December 2008.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-10 is/are pending in the application.
- 4a) Of the above claim(s) 4,9 and 10 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-3 and 5-8 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 03 March 2005 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 4 December 2008 have been fully considered but they are not persuasive. Applicant's arguments have been considered but are moot in view of the new ground(s) of rejection.

The previous rejection of claim 6 under 35 USC 112, 2nd paragraph, is withdrawn. It is clear from the specification that the term "thickness" in this context refers to what is usually referred to as the "width" of the pixel region.

The applicant argues [p. 8] that in the claimed invention differs from *Ohgawara* in that the TFT is turned off and electrically disconnects a data line from the first pixel electrode, so that image data outputted from the data line is not transmitted to the pixel electrode. In contrast, the applicant argues, *Ohgawara* applies a voltage to the peripheral pixels. This is not persuasive. The examiner agrees that *Ohgawara* applies a voltage to the peripheral pixels, but does not agree that *Park* in view of *Ohgawara* does not electrically disconnect the data line from the first pixel electrode by turning the TFT off. This would occur in the normal course of driving the active matrix display, in which the TFTs are repeatedly turned on and off in order to apply and hold the desired voltages on the pixel electrodes.

The amendment to claim 3 raises problems under 35 USC 112.

The previous rejections are therefore maintained, modified as necessary by the amendments to the claims.

Claim Objections

2. Claim 1 is objected to because of the following informalities: "the thin film transistor corresponding to the first area" is without appropriate antecedent, since the TFT is first recited without referring to it being in the first area. Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claim 3 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

See the rejection under 35 USC 112, second paragraph, below. In the event that the second interpretation is the one intended, the specification does not appear to disclose how the direct, permanent electrical connection is made between the pixel electrode and the common electrode (they are on opposite substrates, and such wiring is not indicated in Figs. 5 or 6). How to make and/or use the invention is therefore not disclosed.

Art Unit: 2871

5. Claim 3 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

See the rejection under 35 USC 112, second paragraph, below. In the event that the second interpretation is the one intended, the specification as originally filed does not appear to disclose having a direct, permanent electrical connection made between the pixel electrode and the common electrode (they are on opposite substrates, and such wiring is not indicated in Figs. 5 or 6). Possession of the invention is therefore not disclosed.

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claim 3 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 3 recites "connecting the common electrode and the first pixel electrode". This is unclear. It could mean 1) that they are capacitively connected via Cst or Clc as shown in Figs. 5A-5C, or 2) that there is a permanent, dedicated, physical, essentially zero-resistance electrical connection which is not shown in the figures, or 3) merely that there is an electrical connection through the driving circuitry. In this last case, for

Art Unit: 2871

instance, in Fig. 5A when the gate line is given a voltage to turn on the TFT, the pixel electrode becomes electrically connected with the data line, which can be supplied with the same voltage as the common electrode (in order to produce no electric field across the liquid crystal). In the simplest arrangement, the data line and the common electrode would both be connected to a ground wiring held at the common voltage potential, so the pixel electrode and the common electrode would be connected in this manner. Fig. 5A might be taken to support the first interpretation, of course, but capacitively connecting them would not necessarily form a zero electric field, so it seems unlikely to be the applicant's intent. The line trailing off to the right might suggest the second interpretation, but its purpose does not seem to be described in the specification; the paragraph in the middle of p. 16 of the specification, referring to the grounding of the TFT's gate electrode and also the connection of the pixel electrode and common electrode, might seem to suggest the first or second interpretation. For examining purposes, it is assumed that one of the first or third interpretations, being broader, is intended.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Art Unit: 2871

9. Claims 1-3, 5, and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Park et al.*, US 2002/0113931 in view of *Ohgawara et al.*, U.S. Patent No. 5,617,230.

Park discloses [see Fig. 1a, for instance] a liquid crystal display device comprising: a first substrate [10], a second substrate [20] being opposite to the first substrate; color filters [22] formed on the second substrate; and a liquid crystal layer [30] disposed between the substrates. *Park* discloses a normally black arrangement with TFT [11] (a first thin film transistor formed on the first substrate) supplying a voltage to the pixel electrode [12], so that an electric field is generated between it and the common electrode [23] on the opposite substrate, with the polarizers [14 and 24] aligned so that the pixel becomes dark (light does not pass through) when the electric field is zero [see paragraphs 0034 and 0051, for instance]. *Park* does not disclose the limitations related to the border of the display.

Ohgawara discloses [see Fig. 2, for instance] an analogous liquid crystal display device comprising: a first substrate and a second substrate opposed to the first substrate [see abstract, for instance], a first color filter [17] formed on a first portion [15] of the second substrate, the first portion corresponding to a first area of a display area, the first area being a border area of the display area [see Fig. 2], a second color filter [13] formed on a second portion [11] of the second substrate, the second portion corresponding to a second area of the display area, the second area being the display area except the border area; a first liquid crystal layer [see abstract] disposed between the first and second substrates in the first area, and a second liquid crystal layer

Art Unit: 2871

disposed between the first and second substrates in the second area [see col. 7, line 43—col. 8, lines 15, for instance; note that these are just different portions of the same liquid crystal layer, as in the present specification]. *Ohgawara* also discloses that a voltage is applied in such a manner so as to maintain the peripheral pixels in a light-shielded state [see col. 7, line 43 - col. 8, line 15, for instance], which *Ohgawara* explains can be either a "selective voltage" or a "non-selective voltage" depending on the type of LCD being used. In plainer language, the appropriate voltage is applied to create a dark-state pixel, or to have the liquid crystal in that pixel region act as a closed shutter to prevent light from passing through to the viewer. In the case of *Park*, which is a normally black device, in order to produce the desired light-shielded state, a zero electric field would be formed on the first liquid crystal layer [by applying 0 volts].

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the border arrangement of *Ohgawara* in the device of *Park*, motivated by *Ohgawara's* teaching that this renders the display easier to be seen [see abstract]. In the device of *Park* in view of *Ohgawara*, it would have been obvious to one of ordinary skill in the art at the time of the invention to form the pixel electrodes and TFTs in both the display areas and the border areas, so as to be able to produce a display image and also provide the peripheral light-shielding state taught by *Ohgawara* using *Park's* driving circuitry arrangement, without requiring additional dedicated circuitry. Thus, there would be a first pixel electrode formed on the first substrate corresponding to the first area, a thin film transistor formed on the first substrate corresponding to the first area, and the thin film transistor corresponding to the first area is turned off and

Art Unit: 2871

electrically disconnects a data line from the first pixel electrode [after 0 volts is applied to the pixel electrode via the data line while the TFT is turned on]. Claim 1 is therefore unpatentable.

The zero electric field is formed by nullifying an electric potential difference in the first liquid crystal layer [by applying 0 volts], so claim 2 is also unpatentable. The zero electric field is formed by forming an electrode layer on one of the first and second substrates, the electrode layer making contact with the first liquid crystal layer [see Fig. 1 of *Park*], so claim 5 is also unpatentable. The thickness (width) of the first color filter is no less than a thickness (width) of a pixel unit (region) [see Fig. 2 of *Ohgawara*], so claim 6 is also unpatentable.

In the device of *Park* in view of *Ohgawara*, there is a common electrode formed on the first and second color filter, wherein the first pixel electrode is arranged in a matrix shape [understood to mean that there are other pixel electrodes which together with the first pixel electrode form a matrix] and the zero electric field is formed by setting the common electrode and the first pixel electrode to the same voltage [so there is a 0 volt difference across the liquid crystal layer]. However, it may not be explicitly disclosed that this is done by "connecting" the common electrode and the first pixel electrode. Regarding this last limitation, see the above discussion under 35 USC 112. It would have been obvious to one of ordinary skill in the art at the time of the invention to connect the first pixel electrode and the common electrode (via the TFT, data line, and drive circuitry), in order that they are both conveniently and reliably set to a common reference potential so that the voltage difference between them can be 0 volts

Art Unit: 2871

and there be no electric field in the liquid crystal layer. Claim 3 is therefore unpatentable as well.

10. Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Park et al.*, US 2002/0113931 in view of *Ohgawara et al.*, U.S. Patent No. 5,617,230 as applied above, and further in view of *Takao et al.*, U.S. Patent No. 5,101,289.

Ohgawara discloses [see Fig. 2] that the first color filter comprises three layers [red, green, and blue, for instance], but does not necessarily disclose that each of the three layers has a different thickness from each other.

Takao discloses [see Fig. 3] an analogous LCD having three color filter layers [R, G, and B], each of which has a different thickness from the others. It would have been obvious to one of ordinary skill in the art to do so in the above device, motivated by *Takao's* teaching that the different thicknesses enable the device to obtain desired spectral characteristics [col. 5, lines 42-45], meaning for instance that the hues of the colors can be adjusted to improve the coloration and the quality of the display. Claim 7 is therefore unpatentable.

The limitation of claim 8, that a thickness of the first color filter is regulated by controlling a coating thickness in a process in which the first color filter is coated on the second substrate or by a slit exposure process, is a product-by-process limitation which does not structurally distinguish the claimed device from that of the prior art [see MPEP 2113]. Claim 8 is therefore unpatentable.

Election/Restrictions

11. Claims 4, 9, and 10 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made without traverse in the reply filed on 4 March 2008 and the reply filed on 6 June 2008.

Conclusion

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Art Unit: 2871

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew Schechter whose telephone number is (571) 272-2302. The examiner can normally be reached on Monday - Friday, 9:00 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Andrew Schechter/
Primary Examiner, Art Unit 2871
Technology Center 2800
12 April 2009